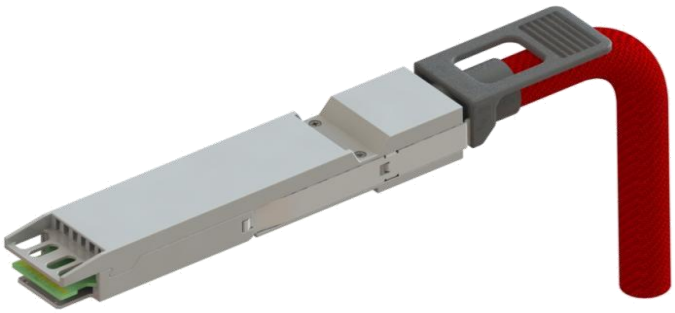
1.6T OSFP1600 TO OSFP1600 Active Direct Attached Cable



FEATURES

- Module compliant to OSFP MSA
- Transmission data rate up to PAM4 212.5Gbps per channel
- Low power consumption
- Linear PAM4 programmable equalizer optimized for 112GBaud copper link up to max length 3M on 26AWG
- Enable Auto-Negotiation and Link Training
- Supports device programming by MCU with I2C
- Power supply 3.3V
- Operating case temperature 0°C to +70°C
- RoHS2.0 compliant

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	-0.3	3.3	3.6	V
Storage temperature	Ts	-40		85	ºC
Operating Case temperature	Tc	0		70	ºC
Humidity	Rh	5		85	%
Data Rate			1600		Gbps

Physical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Length	L	1		3	M
AWG		28		26	AWG
Jacket material		HAIRTAIL Net			

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Power supply voltage	VCC	3.1	3.3	3.5	V
Input LOW Voltage	V_{IL}	-0.3		0.35*V_{CC}	V
Input HIGH Voltage	V_{IH}	0.65* VCC		VCC +0.3	V
Output Logic LOW	V_{OL}			0.25* VCC	V
I2C Master Mode Output Frequency			400		kHz
800G end Power consumption			1.2	1.5	W

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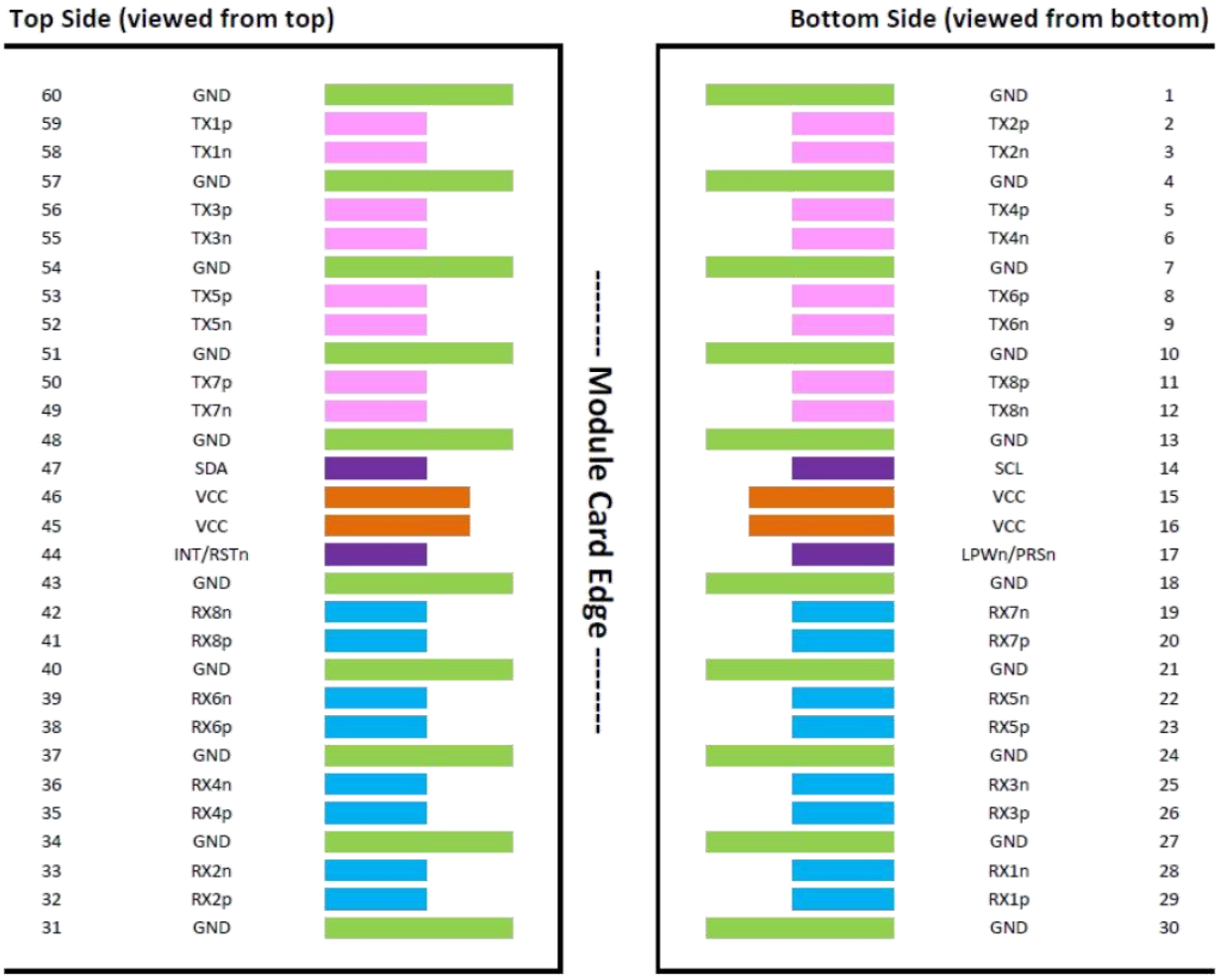
High-Speed Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Raw cable impedance	Zca	90	95	100	ohm
Mated connector Impedance	Zmated	85		110	ohm
Maximum insertion loss at 53.125GHz	SDD21			34	dB
Minimum cable assembly ERL	ERL	8.25			dB
BER				E-8	

Pin Description



Electrical Pin-out Details for OSFP

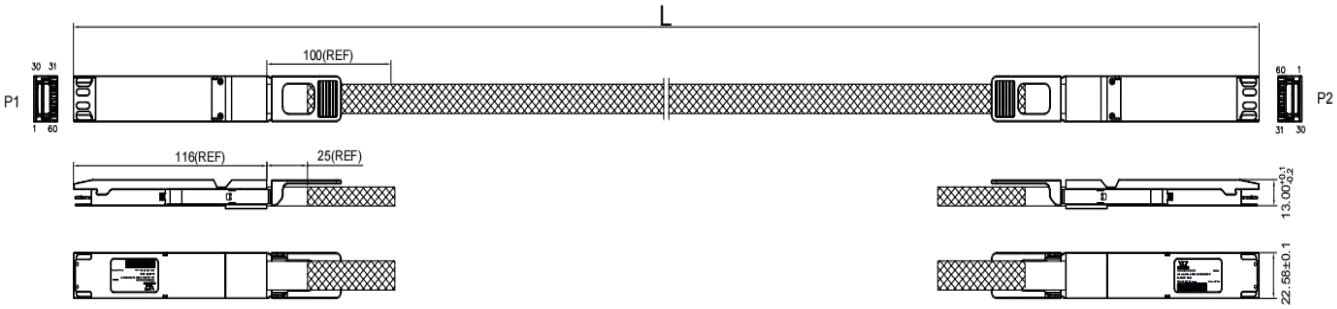
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

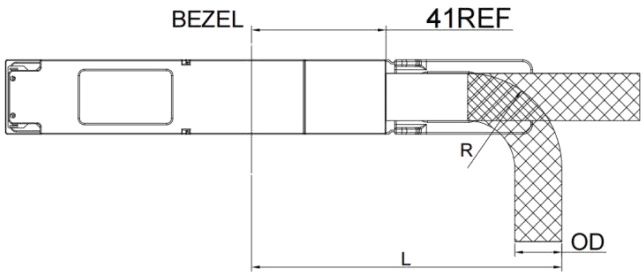
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See pin description for required circuit
45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Module Memory Map

Compatible with CMIS rev 5.0 or further CMIS revisions and customer spec.

Mechanical Dimensions





OSFP TYPE2			
GAUGE	OD	BEND RADIUS "R"	MIN. BEND RADIUS "L"
28AWG	10.2MM	21MM	81MM
26AWG	12.1MM	25MM	86MM

Ordering Information

Model Number Part Number	Description
POOP16CP5	1.6T OSFP1600 to OSFP1600 Active DAC, 0.5M, 28AWG
POOP16C01	1.6T OSFP1600 to OSFP1600 Active DAC,1.0M,28/26AWG
POOP16C1P5	1.6T OSFP1600 to OSFP1600 Active DAC,1.5M, 28/26AWG
POOP16C02	1.6T OSFP1600 to OSFP1600 Active DAC, 2.0M, 28/26AWG
POOP16C03	1.6T OSFP1600 to OSFP1600 Active DAC, 3.0M, 26AWG

References

1. IEEE802.3dj
2. OSFP MSA Rev5.0
3. Common Management Interface Specification (CMIS) Rev5.0

Revision Records

REV.	Description	Designed	Checked	Approved	Issue Date
X1	Preliminary	XICHUN TAN	XICHUN TAN	RYAN LEI	2023.12.18