"Because so much is in your optics"

200G QSFP56 Loopback Module

Features

- Industry's highest rated mating cycles for 2000 and above
- Built-in surge current mitigation technology
- Built-in programmable power dissipation up to 7 W
- Operating temperature: -40℃ to 85℃
- +3.3V power supply
- Supports 10G/25G/56G PAM4 data rates
- 2-wire interface for integrated Digital Diagnostic Monitoring
- Signal integrity performance meets IEEE 802.3ba, 802.3bj, 802.3cd standards respectively
- Custom EEPROM available
- A multi-color LED indicator for high/low power modes
- Hot-pluggable
- RoHS 2.0 compliant

References

- SFF-8665, QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28), Rev 1.8
- SFF-8636, Management Interface for Cabled Environments, Rev 2.9
- SFF-8661, Mechanical requirements specification
- SFF-8679, QSFP28 4X Base Electrical Specification, Rev 1.7
- SFF-8024, SFF Cross Reference to Industry Products, Rev 4.4

Ordering Information

Part Number	Product Description
POQP20LP-7	QSFP56 200G LOOPBACK ,7W, WHITE PULLTAB, Compliance with SFF-8636
POQP20LP-3.5	QSFP56 200G LOOPBACK ,3.5W, ORANGE PULLTAB, Compliance with SFF-8636
POQP20LP-0	QSFP56 200G LOOPBACK ,0W, BLACK PULLTAB, Compliance with SFF-8636

Description

Designed and engineered to accommodate customers high usage 2000 cycles at -40°C to 85°C, the loopback module series are the most reliable products in the market to enable the quickest customers systems production and deployment. Software defined multiple power consumption may emulate the optical module power, and the embedded insertion loss characteristics emulates the real-world cabling for 40G/100G/200G Ethernet/Infiniband/FC. The built-in surge current mitigation technology mitigates the DUT risks from being damaged. The broad operating temperature range accommodates the enterprise, datacom and telecom applications. The loopback module may be used for ports testing, field deployment testing and equipment troubleshooting.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Storage Temperature	Tst	-40	+85	ºC
Operating Case Temperature	Tc	-40	+85	ºC
Storage Relative Humidity	RH_S	0	95	%
Operating Humidity	RHo	0	85	%
Supply Voltage	Vcc	2.97	3.63	V

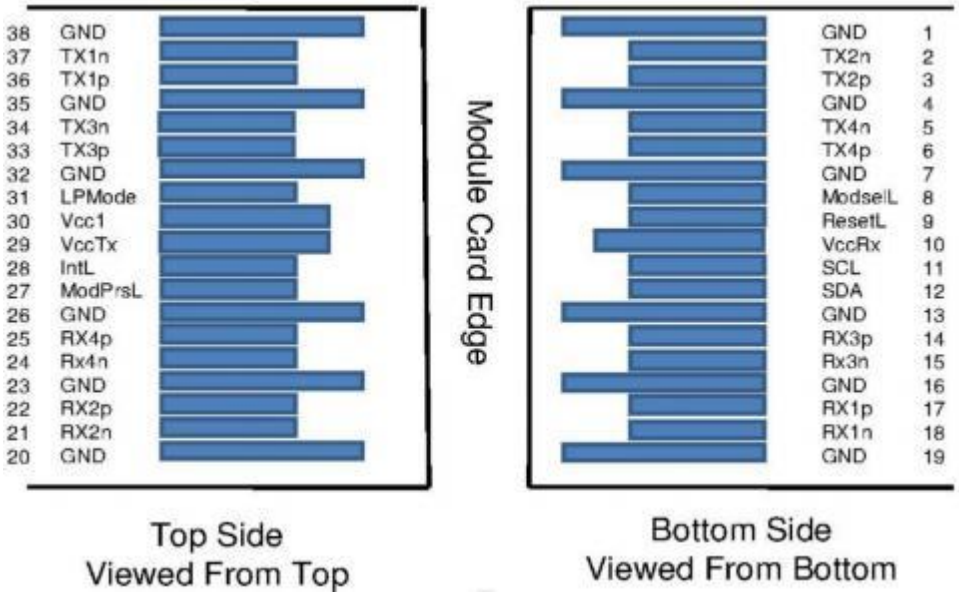
Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case temperature	Tc	-40	-	85	ºC
Supply Voltage	Vcc	2.97	3.3	3.63	V
Data Rate	BRate	0.1	-	200	Gbps
Durability Cycles		-	2000	2250	Cycles

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential input impedance	Zin	90	100	110	ohm	
Insertion Loss@14GHz	SDD21	3.5	-	10	dB	The insertion loss for TX to RX, including the AC Caps, as measured with MCB,The MCB insertion loss comply with IEEE 802.3bj CL92.11.2
Insertion Loss Deviation	ILD	-1		1	dB	At Nyquist Frequency
Return Loss		IEEE 802.3bj CL92.10.3.				
Skew between lanes	SKEW			200	ps	
Clock Frequency	f_{SCL}	0		400	KHz	
Clock Stretching	T_clock_hold			500	μs	

Pin Description



Top Side
Viewed From Top

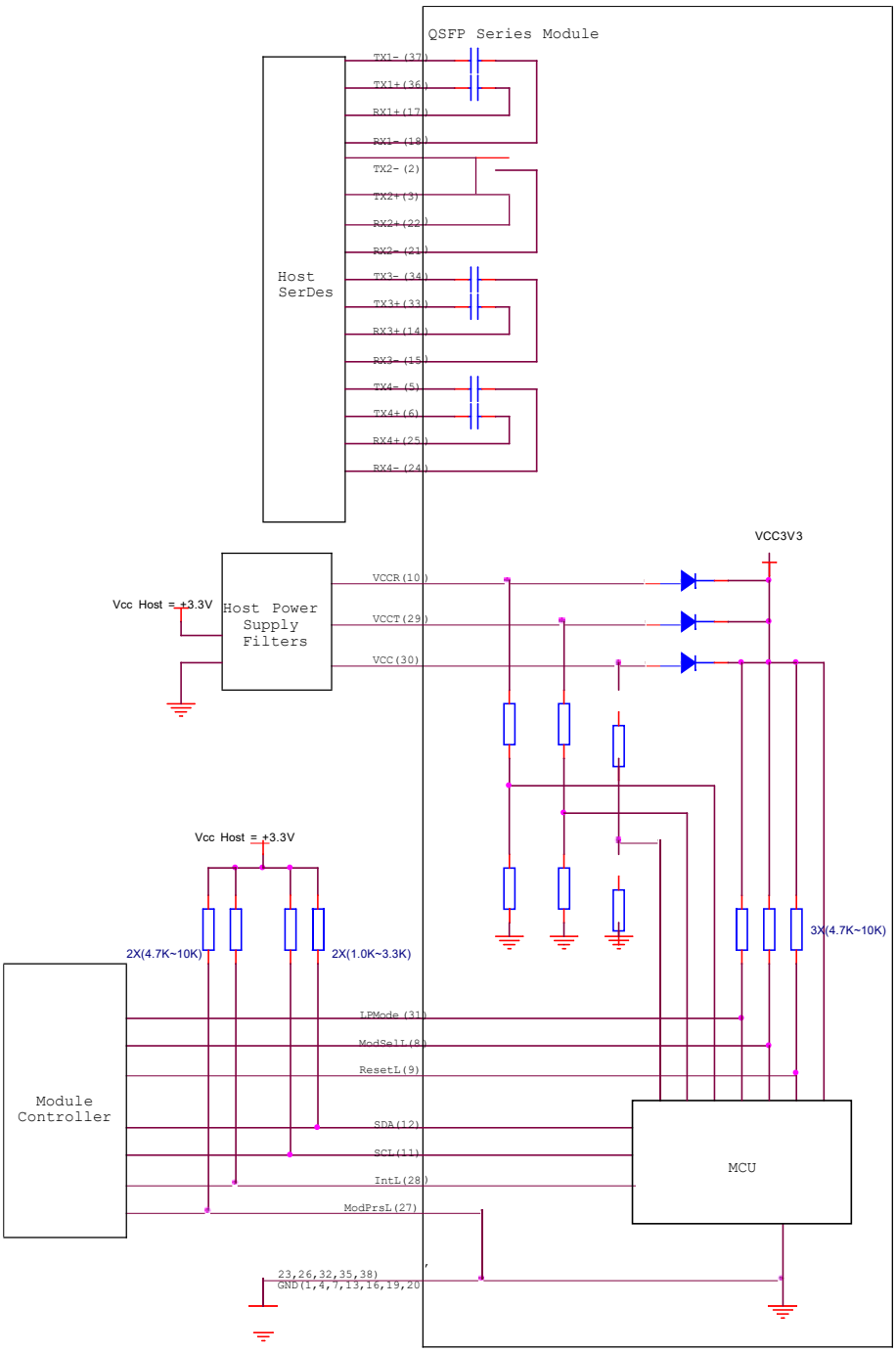
Bottom Side
Viewed From Bottom

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Typical application Circuit

The 8 lanes are connected as following with match polarity:

- TX1 and RX1
- TX2 and RX2
- TX3 and RX3
- TX4 and RX4



QSFP56 Register access

All the other registers defined in the SFF-8636, Management Interface for Cabled Environments, Rev 2.9 may be optional.

QSFP56 Identification

The module must provide the ID in the following registers

Page	Address	Size	Name	Description
N/A	0	1	Identifier	11h : Identifier Type for QSFP28
N/A	2	1	Data_Not_Ready	b0000_0xx0: Data_Ready
00h	128	1	Identifier	11h : Identifier Type for QSFP28
	148-163	16	Vendor name	Vendor name (ASCII)
	168-183	16	Vendor PN	Part number provided by vendor (ASCII)
	184-185	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
	196-211	16	Vendor SN	Vendor Serial Number (ASCII)
03h	130-131	2	Temperature Low Alarm	Temperature Range
N/A	93	1	Maximum Power identifier	bxxxx_00xx: 0-Watt loopback(Without Power burner) bxxxx_01xx: 3.5-Watt loopback bxxxx_10xx: 7-Watt loopback

QSFP56 loopback ID registers

Case temperature monitor

The Case temperatures should be monitored on both top and bottom of the case specified below:

Page	Address	Size	Name	Description
N/A	22	1	Temperature MSB (Top case Temperature MSB)	Internally measured temperature, top case: signed 2's complement in 1/256 °C increments NOTE: Temperature can be below 0°C.
	23	1	Temperature LSB (Top case Temperature LSB)	
	24	1	Reserved (Bottom case Temperature MSB)	Internally measured temperature, bottom case: signed 2's complement in 1/256 °C increments NOTE: Temperature can be below 0°C.
	25	1	Reserved (Bottom case Temperature LSB)	
Page	**Address**	**Bits**	**Name**	**Description**
N/A	6	7	Top TempMonHighAlarmFlag	Latched Flag for Top High temperature Alarm
		6	Top TempMonLowAlarmFlag	Latched Flag for Top Low temperature Alarm
		5	Top TempMonHighWarningFlag	Latched Flag for Top High temperature Warning
		4	Top TempMonLowWamingFlag	Latched Flag for Top Low temperature Warning
		3	Bottom TempMonHighAlarmFlag	Latched Flag for Bottom High temperature Alarm

		2	Bottom TempMonLowAlarmFlag	Latched Flag for Bottom Low temperature Alarm
		1	Bottom TempMonHighWarningFlag	Latched Flag for Bottom High temperature Warning
		0	Bottom TempMonLowWamingFlag	Latched Flag for Bottom Low temperature Warning

Power rail voltage monitor

The 3 VCC power rails, VccRx, VccTx and Vcc1 are monitored individually.

VCC voltage DOM

Page	Address	Size	Name	Description
N/A	26	1	Supply Voltage MSB (VccRx voltage LSB)	Internally measured 3.3 volt input supply voltage VccRx: in 100μV increments
	27	1	Supply Voltage MSB (VccRx voltage LSB)	
	28	1	Reserved (V cc Tx voltage MSB)	Internally measured 3.3 volt input supply voltage VccTx: in 100μV increments
	29	1	Reserved (V cc Tx voltage LSB)	
	30	1	Vendor Specific (Vcc1 voltage MSB)	Internally measured 3.3 volt input supply voltage Vcc1: in 100μV increments
	31	1	Vendor Specific (Vcc1 voltage LSB)	

Page	Address	Bits	Name	Description
N/A	7	7	VccRx MonHighAlarmFlag	Latched Flag for High supply VccRx voltage Alarm
		6	VccRx MonLowAlarmFlag	Latched Flag for Low supply VccRx voltage Alarm
		5	VccRx MonHighWarningFlag	Latched Flag for High supply VccRx voltage Warning
		4	VccRx MonLowWarningFlag	Latched Flag for Low supply VccRx voltage Warning
		3	VccTx MonHighAlarmFlag	Latched Flag for High supply VccTx voltage Alarm
		2	VccTx MonLowAlarmFlag	Latched Flag for Low supply VccTx voltage Alarm
		1	VccTx MonHighWarningFlag	Latched Flag for High supply VccTx voltage Warning
		0	VccTx MonLowWarningFlag	Latched Flag for Low supply VccTx voltage Warning
	8	7	Vcc MonHighAlarmFlag	Latched Flag for High supply Vcc voltage Alarm
		6	Vcc MonLowAlarmFlag	Latched Flag for Low supply Vcc voltage Alarm
		5	Vcc MonHighWarningFlag	Latched Flag for High supply Vcc voltage Warning
		4	Vcc MonLowWarningFlag	Latched Flag for Low supply Vcc voltage Warning

Status LED

A multi-color LED must be viewed from the front of the module in order to signify high/low power modes, as well as interrupts. Low-power mode is defined as device address A0h.93.7:4 = 0000b or The LPMode is High.

- Solid green: low-power mode
- Solid red: high-power mode
- Blinking green: low-power mode with any of the interrupt flag is set
- Blinking red: high-power mode with any of the interrupt flag is set

I2C interface

Upon the completion of the MgmtInit state, the I2C interface on the module must support Fastmode as defined in the UM10204, I2 C-bus specification and user manual, Rev. 6 – 4 April 2014 in order to handle the SCL clock frequency between 0kHz and 400KHz. In addition, the module may only clock stretching the SCL less than 100 µsec in any frequency.

Reset requirement

There should be 3 different type of reset in the module, power-up-reset, hard-reset[1] and softreset[2].

Power-up-reset

The power-up-reset should cause all the active components, including the microcontroller, in the module reset to default state and then start the normal operation. It should also reset the power burner in the module to consume the default power, 1.5W.

Hard-reset(ResetL)

The hard-reset should cause the microcontroller to reset, and then reset all the other active components and reset the power burner to consume the default power, 1.5W. Afterward, the microcontroller will start the normal operation.

Soft-reset

The soft-reset should cause the microcontroller to reset, and then reset all the other active components and reset the power burner to consume the default power, 1.5W. Afterward, the microcontroller will start the normal operation. The soft-reset is set by host through the I2C register 32 and 33.

Page	Address	Bits	Name	Description	Type
N/A	32	8	Software Reset	Software reset will be executed when the following value are written: Byte 32 : 0xFA Byte 33 : 0xCE	RW, Self-Clear
	33	8			

Notes:

1. Hard-reset is referred to the ResetL signal.
2. Soft-reset is referred to the Software reset bytes in the I2C address 32 and 33.
3. The soft-reset is defined in loopback module only.

Digital state detection and report on LPMode and ModSelL

The module is able to detect the digital state of the LPMode and ModSelL signals,

Page	Address	Bits	Name	Description	Type
FFh	225	5	ModSelL transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
		4	LPMode transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW

ModSelL

The ModSelL is Low, the module responds to TWI serial communication commands.

The ModSelL is High, the module shall not respond to or acknowledge any TWI interface communication.

LPMode

The LPMode is Low, the power burner in the module to consume the setting power.

The LPMode is High, the module enter low power mode.

ModPrsL

The ModPrsL is pulled towards ground in the module.

IntL

The IntL signal is asserted Low with any of Alarm and Warning flag is set and deasserted High after all of Alarm and Warning flags are read.

Programmable power consumption/burner

During power-up of the module, the power burner in the module should burn maximum 1.5W power as default. Afterward, host can set the module to consume more power through a I2C register 93.

Page	Address	Bits	Name	Description	Type
N/A	93	7-5	Reserved (Power Controller)	00xb: Power consumption: 1.5W (default) 01xb: Power consumption: 2.5W 100b: Power consumption: 3.5W 101b: Power consumption: 4.0W 110b: Power consumption: 4.5W 111b: Power consumption: 5.0W The tolerance of power consumption must meet the following criteria : +/-5% @ VCC = 3.3V +/-2% +/-11% @ VCC = 3.3V +/-5% +/-20% @ VCC = 3.3v +/-10%	RW
		4	Reserved (Maximum power controller)	0b: Power consumption is set by the Power Controller register (default) 1b: Power consumption: 7.0W	RW
		3-2	Maximum power identifier	00b: 0-Watt loopback 01b: 3.5-Watt loopback 10b: 7-Watt loopback	RO
		1-0	High Power Class enabled	00b	RO

Contact pads insertion requirement and module reliability

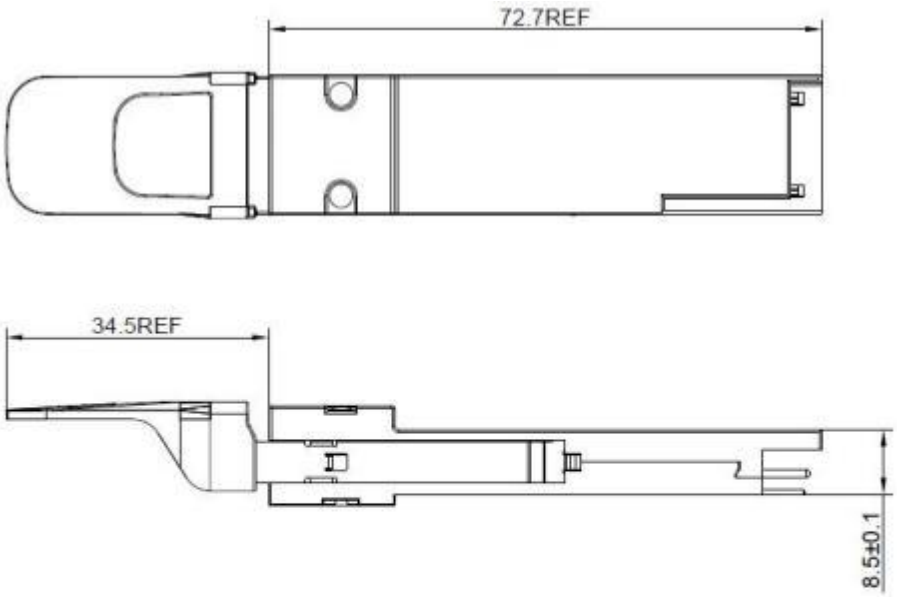
The value of guaranteed maximum insertion/temperature cycle must be saved in I2C registers in upper page 0xFF

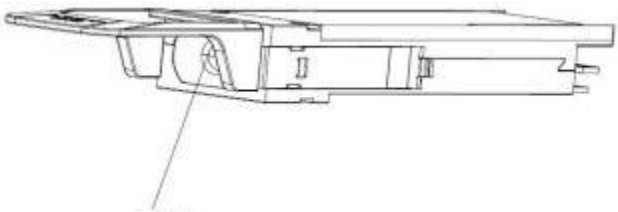
Contact pads insertion cycle registers

Page	Address	Size	Name	Description	Type
FFh	252	1	Guaranteed maximum insertion/temperature cycle, MSB	Guaranteed maximum insertion/temperature cycle in hex. The goal is 2000 (07D0h) insertions.	RO
	253	1	Guaranteed maximum insertion/temperature cycle, LSB		RO

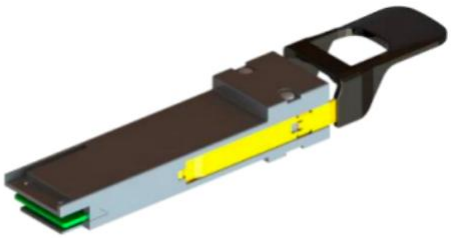
Package Outline

Dimensions are in millimeters. (Unit: mm)

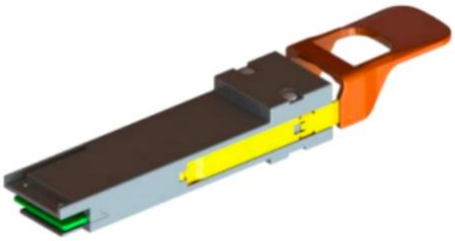




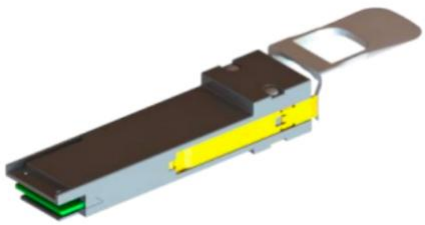
LED:
Solid green: low-power mode
Solid red: high-power mode
Blinking green: low-power mode with any of the interrupt flag is set
Blinking red: high-power mode with any of the interrupt flag is set



0- Watt



3.5-Watt



7-Watt