800G QSFP-DD Loopback Module (Straight-mapping)

Features

- Industry's highest rated mating cycles for 2000 and above
- Built-in surge current mitigation technology
- Adjustable total power consumption up to 30W distributed to the 3 regions, each region is individually programmed between 1.0W through 10.0W with 0.5W increment
- Operating temperature: -40℃ to 85℃
- +3.3V power supply
- Supports 8* 10G/25G/56G PAM4/112G data rates
- 2-wire interface for integrated Digital Diagnostic Monitoring
- Signal integrity performance meets IEEE 802.3bj, 802.3cd，802.3ck standards respectively
- Enhanced EMC/EMI design for noise harsh environment
- Enhanced heat dissipation technology for high power testing
- Custom EEPROM available
- A multi-color LED indicator for high/low power modes
- Hot-pluggable
- RoHS 2.0 compliant

Application

- QSFP-DD port/system testing
- Ethernet IEEE 802.3 (Gigabit, 10 Gigabit and 25 Gigabit Ethernet)
- SONET, SDH, GBE, Fiber Channel Support

Standard

- Common Management Interface Specification, Rev 4.0
- QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification, Rev 6.01
- IEEE Std 802.3cd
- IEEE Std 802.3ck Draft 3.0
- IEEE 802.3cd
- IEEE 802.3bj
- SFF-8024, SFF Cross Reference to Industry Products, Rev 4.7

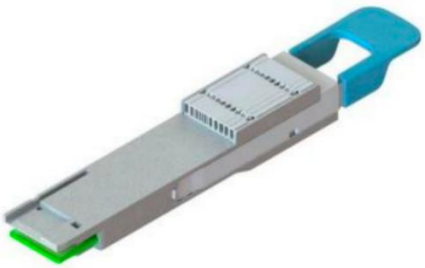
Straight-mapping

The 16 lanes are connected as following with match polarity:

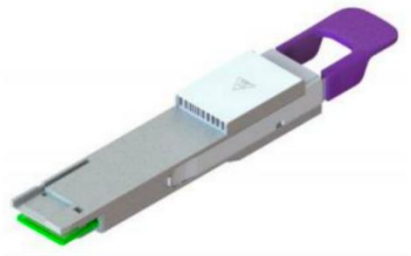
- TX1 and RX1
- TX2 and RX2
- TX3 and RX3
- TX4 and RX4
- TX5 and RX5
- TX6 and RX6
- TX7 and RX7
- TX8 and RX8

Ordering Information

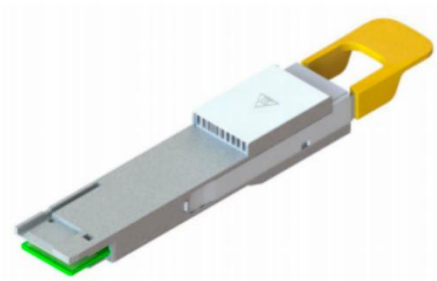
Part Number	Product Description
POQD80LP-0	QSFP-DD 2A 800G Loopback 0W ,Straight-mapping, BLUE Pull-Tab,Compliance with CMIS
POQD80LP-16	QSFP-DD 2A 800G Loopback 16W ,Straight-mapping, PURPLE Pull-Tab,Compliance with CMIS
POQD80LP-24	QSFP-DD 2A 800G Loopback 24W ,Straight-mapping, ORANGE Pull-Tab,Compliance with CMIS
POQD80LP-30	QSFP-DD 2A 800G Loopback 30W ,Straight-mapping, GREEN Pull-Tab,Compliance with CMIS



0-Watt



16-Watt



24-Watt

30-Watt

Description

Designed and engineered to accommodate customers high usage 2000 cycles from -40°C to 85°C, the loopback module series are the most reliable products in the market to enable the quickest customers systems production and deployment. Software defined multiple power consumption may emulate the optical module power, and the embedded insertion loss characteristics emulates the real-world cabling for 100G/400G/800G Ethernet/Infiniband/FC. The built-in surge current mitigation technology mitigates the DUT risks from being damaged. The broad operating temperature range accommodates the enterprise, datacom and telecom applications. The loopback module may be used for ports testing, field deployment testing and equipment troubleshooting.

Specification

Absolute Maximum Ratings				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Storage Temperature	Ts	-40	+85	℃
Ambient Operating Temperature	Ta	-40	+85	℃
Storage Relative Humidity	RH_S	0	95	%
Operating Relative Humidity	RH_O	0	85	%
Power Supply Voltage	Vcc	2.97	+3.63	V

Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
Ambient Operating Temperature	Ta	-40	-	+85	℃
Power Supply Voltage	V_{CC}	2.97	3.3	3.63	V
Data Rate	BRate	0.1	-	800	Gbps
Durability Cycles		-	2000	2250	Times

High Speed Characteristics						
Parameter	**Symbol**	**Min**	**Typical**	**Max**	**Unit**	**Notes**
Input/Output Impedance	Zd	90	95	105	Ohm	Differential Impedance
Return Loss	SDD11/22	<-10 <-5	0.01GHz ≤ f < 10GHz 10GHz≤ f < 40GHz		dB	

Insertion Loss	SDD21	-	-	7 (Include Trace&Via&Mating& Connectors，Without MCB insertion loss)	dB	The insertion loss for TX to RX, including the AC Caps, as measured with MCB,The MCB insertion loss comply with IEEE 802.3ck CL 162B.1.2.1
				11.75 (Include MCB insertion loss&Trace&Via& Mating&Connectors)		
Intra Pair Skew	IPS			100	ps	

Pin Definition

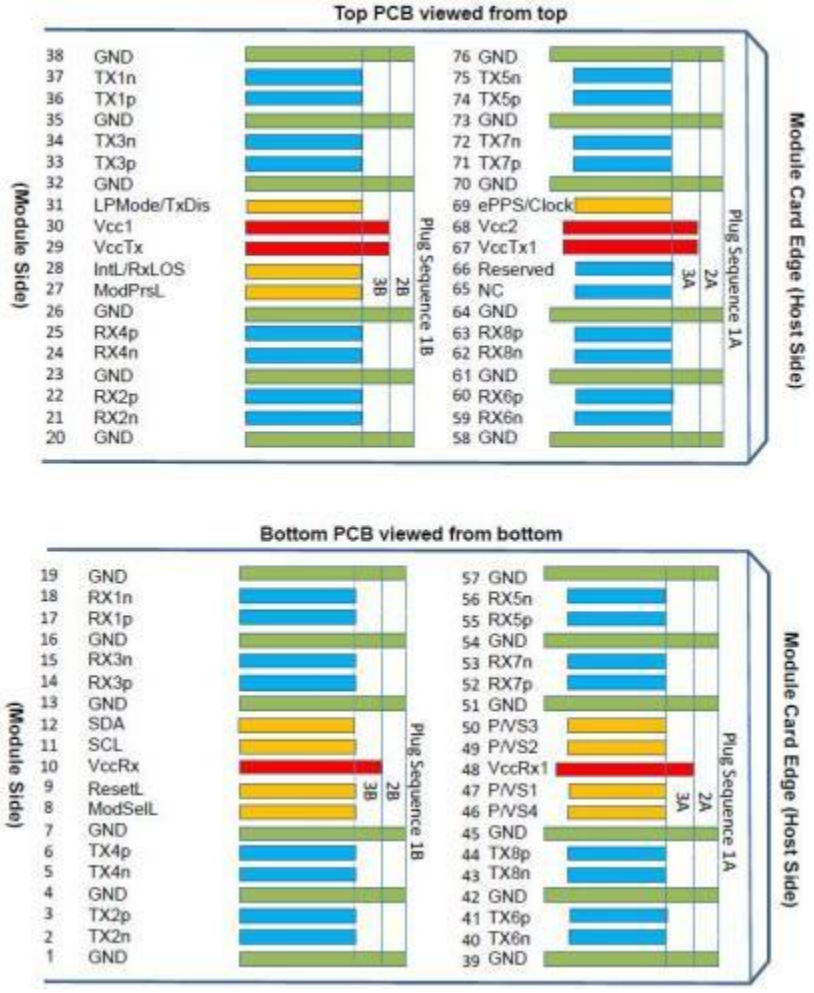


Table 1- Pad Function Definition

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3B	
12	LVCMOS-I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is rated for a steady state current of 500 mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13. For power classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.

Note 3: Reserved pad recommended to be terminated with 10 kΩ to ground on the host. Pad 65 (No Connect) Shall be left unconnected within the module, optionally pad 65 may get terminated with 10 kΩ to ground on the host.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (See Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B, followed by 3A and 3B.

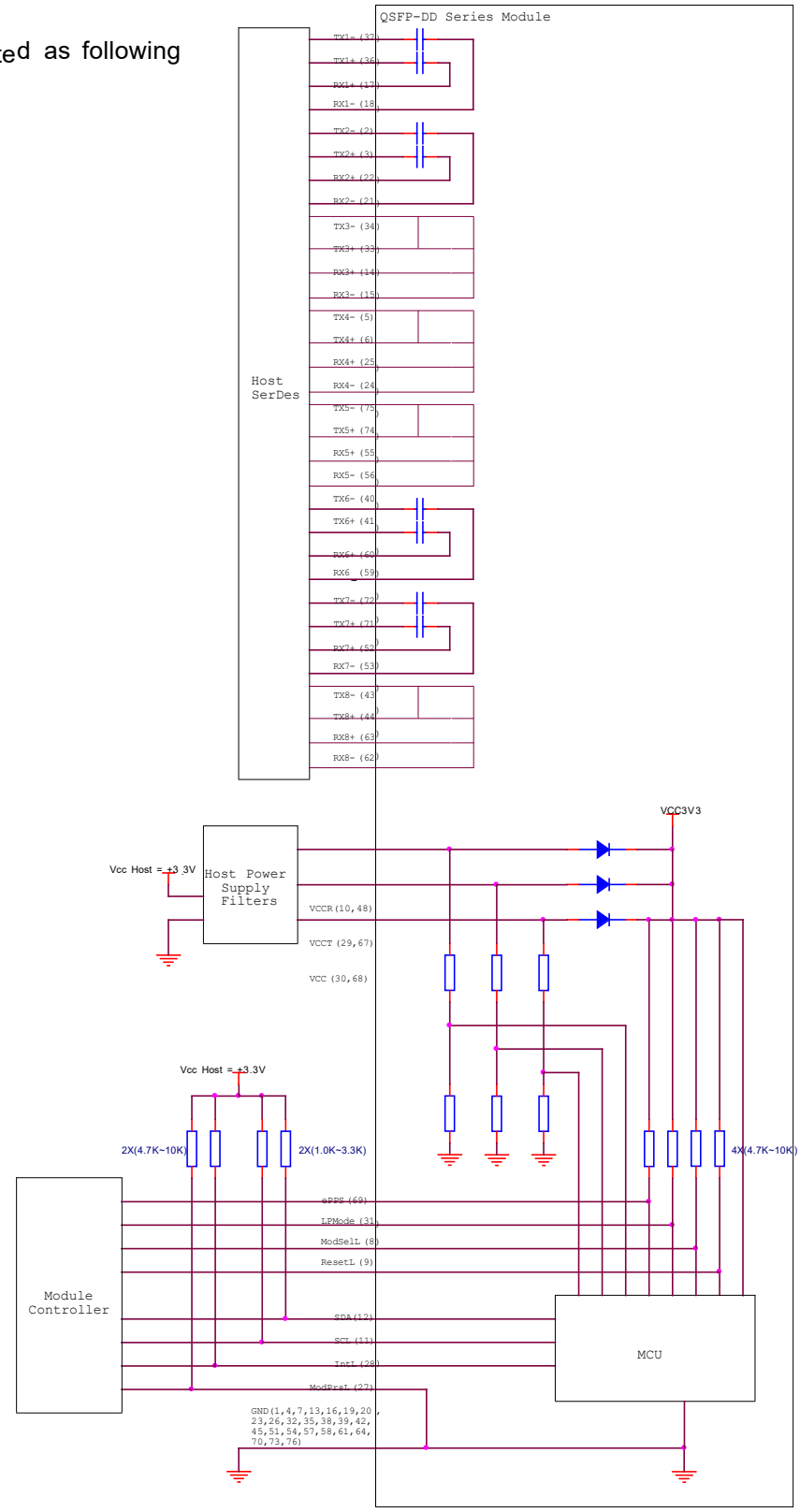
Note 5: Full definitions of the P/VSx signals currently under development. For module designs using programmable/vendor specific inputs P/VS1 and P/VS4 signals it is recommended each to be terminated in the module with 10 kΩ. For host designs using programmable/vendor specific outputs P/VS2 and P/VS3 signals it is recommended each to be terminated on the host with 10 kΩ.

Note 6: for host not implementing ePPS/Clock, it is not necessary to parallel terminate the ePPS/Clock signal to ground on the host. ePPS/Clock already has parallel termination in the module see 4.2.6.

Typical application Circuit

The 16 lanes are connected as following with match polarity:

- TX1 and RX1
- TX2 and RX2
- TX3 and RX3
- TX4 and RX4
- TX5 and RX5
- TX6 and RX6
- TX7 and RX7
- TX8 and RX8



Status LED

A multi-color LED must be viewed from the front of the module in order to signify high/low power modes, as well as interrupts .Low-power mode is defined as device address A0h.00.200.6:4 = 000b or The LPMode is High.

- Solid green: low-power mode
- Solid red: high-power mode
- Blinking green: low-power mode with any of the interrupt flag is set
- Blinking red: high-power mode with any of the interrupt flag is set

I2C interface

Upon the completion of the MgmtInit state, the I2C interface on the module must support Fast-mode as defined in section 4.5.1 of the QSFP-DD/QSFP-DD800/QSFP112 Hardware Specification, Rev 6.01 in order to handle the SCL clock frequency between 0kHz and 400KHz. In addition, the module may only clock stretching the SCL less than 100 μsec in any frequency.

NVRAM

A 128-byte NVRAM be accessed through I2C:

The NVRAM be located at page 0x03 address 128 through address 255.

The NVRAM support Current Address Read Operation, Random Read Operation , Sequential Bytes Read Operation, Byte Write Operation6 and Sequential Bytes Write Operation .

The NVRAM support Fast-mode as defined in section 4.5.1 of the QSFPDD/QSFP-DD800/QSFP112 Hardware Specification, Rev 6.01.

The default value in the NVRAM is 00h for the entire 128 bytes

QSFP-DD Identification:

Table 1: loopback ID registers

Page	Address	Size	Name	Description
N/A	0	1	Identifier	18h: Identifier Type of QSFP-DD
	3	1	Module state	b0000_011x: ModuleReady state.
	85	1	Module Type Encodings	0x03: Passive Cu
	86	1	ApSelCode 1: Host Electrical Interface Code	0x49: 800GBASE-CR8
	87	1	ApSelCode 1: Module Media Interface Code	0xBF: Passive Loopback Module
00h	128	1	Identifier	18h: Identifier Type of QSFP-DD

	129-144	16	Vendor name	Vendor name (ASCII)
	148-163	16	Vendor PN	Part number (ASCII)
	164-165	2	Vendor rev	Revision (ASCII)
	166-181	16	Vendor SN	Vendor Serial Number (ASCII)
	200	1	Maximum Power identifier	bxxxx_01xx: 30-Watt loopback bxxxx_101x: 24-Watt loopback bxxxx_00xx: 16-Watt loopback bxxxx_11xx: 0-Watt loopback Refer to address 201
	201	1	Max Power	0x78 (30W/0.25W = 120) 0x60 (24W/0.25W = 96) 0x40 (16W/0.25W = 64) 0x00 :(0W,Without Power burner. Only EEPROM)

Table 2: QSFP-DD loopback non-ID registers:

Page	Address	Size	Name	Description
N/A	12-15	4	Temperature DOM	Refer to Table 3
	16-19, 22-23	6	Voltage DOM	Refer to Table 4
	26	1	Self-reset	Refer to Table 5
00h	200	bit 6-4	Power burner control	Refer to Table 6
	214-216	3	Power burner setting	Refer to Table 6
03h	128-255	128	NVRAM	
FFh	225	bit 6,2-1	Low-Speed Signal Status	Refer to Table 7
		bit 7,5-4	Low-Speed Signal state transaction	Refer to Table 8
	250-251	2	Power-cycle counter	Refer to Table 11
	252-253	2	Contact pads insertion cycle	Refer to Table 12

Case temperature monitor

The Case temperatures is monitored on the top of the case.

Table 3: temperature DOM

Page	Address	Size	Name	Description
N/A	12	1	Reserved / Temperature 2 MSB	Internally measured temperature, top case: signed 2's complement in 1/256°C increments
	13	1	Custom / Temperature 2 LSB	

	14	1	Module Monitor 1: Temperature 1 MSB	Internally measured temperature, top case: signed 2's complement in 1/256°C increments
	15	1	Module Monitor 1: Temperature 1 LSB	
Page	**Address**	**Bits**	**Name**	**Description**
N/A	9	3	TempMonLowWamingFlag	Latched Flag for low temperature warning
		2	TempMonHighWarningFlag	Latched Flag for high temperature warning
		1	TempMonLowAlarmFlag	Latched Flag for low temperature alarm
		0	TempMonHighAlarmFlag	Latched Flag for high temperature alarm

Power rail voltage monitor

The 3 VCC power rails, VccRx*, VccTx* and Vcc* are monitored individually.

Table 4: VCC voltage DOM

Page	Address	Size	Name	Description
N/A	16	1	Module Monitor 2: Supply 3.3-volt MSB	Internally measured 3.3 volt input supply voltage VccRx* gold-fingers: in 100μV increments
	17	1	Module Monitor 2: Supply 3.3-volt LSB	
	18	1	Module Monitor 3: Supply 3.3-volt MSB	Internally measured 3.3 volt input supply voltage VccTx* gold-fingers: in 100μV increments
	19	1	Module Monitor 3: Supply 3.3-volt LSB	
	22	1	Module Monitor 5: TEC current MSB	Internally measured 3.3 volt input supply voltage Vcc* gold-fingers: in 100μV increments
	23	1	Module Monitor 5: TEC current MSB	
Page	**Address**	**Bits**	**Name**	**Description**
N/A	9	7	VccRx MonLowWarningFlag	Latched Flag for low supply VccRx voltage warning
		6	VccRx MonHighWarningFlag	Latched Flag for high supply VccRx voltage warning
		5	VccRx MonLowAlarmFlag	Latched Flag for low supply VccRx voltage alarm
		4	VccRx MonHighAlarmFlag	Latched Flag for high supply VccRx voltage alarm
	10	3	VccTx MonLowWarningFlag	Latched Flag for low supply VccTx voltage warning
		2	VccTx MonHighWarningFlag	Latched Flag for high supply VccTx voltage warning

		1	VccTx MonLowAlarmFlag	Latched Flag for low supply VccTx voltage alarm
		0	VccTx MonHighAlarmFlag	Latched Flag for high supply VccTx voltage alarm
	11	3	Vcc MonLowWarningFlag	Latched Flag for low supply Vcc voltage warning
		2	Vcc MonHighWarningFlag	Latched Flag for high supply Vcc voltage warning
		1	Vcc MonLowAlarmFlag	Latched Flag for low supply Vcc voltage alarm
		0	Vcc MonHighAlarmFlag	Latched Flag for high supply Vcc voltage alarm

Reset requirement

There are 3 different type of reset in the module, power-up-reset, hard-reset and soft-reset. All the 3 resets should cause the module to consume default power: less than 1.5W.

Power-up-reset

The power-up-reset should cause all the active components, including the microcontroller, in the module reset to default state and then start the normal operation. It should also reset the power burner in the module to consume the default power.

Hard-reset(ResetL)

The hard-reset should cause the microcontroller to reset, and then reset all the other active components and reset the power burner to consume the default power. Afterward, the microcontroller will start the normal operation.

Soft-reset

The soft-reset should cause the microcontroller to reset, and then reset all the other active components and reset the power burner to consume the default power. Afterward, the microcontroller will start the normal operation. The soft-reset is set by host through the I2C register 26 bit 3.

Table 5: Soft-reset register

Page	Address	Bits	Name	Description	Type
N/A	26	3	Software Reset	Software reset	RW, Self-Clear

Programmable power consumption/burner

During power-up of the module, the default power consumption in the module should burn less than 0.5W to boot up the MCU and associated control logic/circuitry as default. Afterward, host can set the module to consume higher power by programming the 3 burners in 3 regions through I2C registers 200, 214-216 when the LPMode is Low.

Table 6: power burner registers

Page	Address	Bits	Name	Description	Type
00h	200	7	Reserved	0b	RO
		6	Region 3 burner	The burner in each region is individually enabled by these bits. 0b: Disable (default) 1b: Enable	RW
		5	Region 2 burner		
		4	Region 1 burner		
		3-0	Maximum Power identifier	bxxxx_01xx: 30-Watt loopback bxxxx_101x: 24-Watt loopback bxxxx_00xx: 16-Watt loopback bxxxx_11xx: 0-Watt loopback Refer to address 201 (or Customizable power)	RO
	213	7-0	Reserved	00b	RO
	214	7-0	Region 3 power consumption	The power in each region is individually programmed between 1.0W through 10.0W 10h: 1.0W (default) 18h:1.5W 20h: 2.0W 28h: 2.5W 30h: 3.0W 38h: 3.5W 40h: 4.0W 48h: 4.5W 50h: 5.0W 58h: 5.5W 60h: 6.0W 68h: 6.5W 70h: 7.0W 78h: 7.5W 80h: 8.0W 88h: 8.5W 90h: 9.0W 98h: 9.5W A0h: 10.0W Else: remain the current value. The tolerance of power consumption must meet the following criteria : +/-5% @ VCC = 3.3V +/-2% +/-11% @ VCC = 3.3V +/-5% +/-20% @ VCC = 3.3v +/-10%	RW
	215	7-0	Region 2 power consumption		RW
	216	7-0	Region 1 power consumption		RW

Power distribution

The power burner is placed on the top side of paddle PCB with all the heat be dissipated at the top of the case. The power burner is separated into 3 regions as shown:

Each region can be individually enabled by register 200 and programmed the amount of power consumption by corresponding registers between 214 and 216.

- The sub-region x.1 should dissipate 75% of the power from the corresponding region
- The sub-region x.2 should dissipate 25% of the power from the corresponding region.
- Each region will be driven by a single power rails as defined below:
  - Region 1: VccTx*,
  - Region 2: VccRx*,
  - Region 3: Vcc*

Table 7: Low-Speed Signal status registers

Page	Address	Size	Name	Description	Type
FFh	225	6	ePPS signal status	0b: logical 0, $V_{ePPS} < V_{il}$(max) 1b: logical 1, $V_{ePPS} > V_{ih}$(min)	RO
		2	ModSelL signal status	0b: logical 0, $V_{ModSelL} < V_{il}$(max) 1b: logical 1, $V_{ModSelL} > V_{ih}$(min)	RO
		1	LPMode signal status	0b: logical 0, $V_{LPMode} < V_{il}$(max) 1b: logical 1, $V_{LPMode} > V_{ih}$(min)	RO

Table 8: Low-Speed Signal state transaction registers

Page	Address	Size	Name	Description	Type
FFh	225	7	ePPS transition	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
		5	ModSelL transition	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
		4	LPMode transition	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW

ModSelL

The ModSelL is Low, the module responds to TWI serial communication commands.

The ModSelL is High, the module shall not respond to or acknowledge any TWI interface communication.

LPMode

The LPMode is Low, the power burner in the module to consume the setting power.

The LPMode is High, the module enter low power mode.

ModPrsL

The ModPrsL is pulled towards ground in the module.

IntL

The IntL signal is asserted Low with any of Alarm and Warning flag is set and deasserted High after all of Alarm and Warning flags are read.

Table 9: Alarm and Warning Thresholds(Page 02H Byte 128~143)

Page	Address	Size	Name of field	Description
02h	128-129	2	Temp High Alarm	MSB at low address, 95℃
	130-131	2	Temp Low Alarm	MSB at low address, -10℃
	132-133	2	Temp High Warning	MSB at low address, 85℃
	134-135	2	Temp Low Warning	MSB at low address, -5℃
	136-137	2	VCC Voltage High Alarm	MSB at low address, 3.6V
	138-139	2	VCC Voltage Low Alarm	MSB at low address, 3.0V
	140-141	2	VCC Voltage High Warning	MSB at low address, 3.5V
	142-143	2	VCC Voltage Low Warning	MSB at low address, 3.1V

PS: Alarm and Warning Thresholds can be customized according to customer requirements

Power-cycle counter

Every time the MCU in the module is powered-up, the power-cycle counter will be implemented. The default value of the counter is 00_00h. The value of the counter must be saved in I2C registers in Page FFh.

Table 10: Power-cycle counter registers

Page	Address	Size	Name	Description	Type
FFh	250	1	Power-cycle counter, MSB	Power-cycle counter. Default to 00_00h from factory.	RO
	251	1	Power-cycle counter, LSB		RO

Contact pads insertion requirement and module reliability

The contacts pads on the paddle card is maintain the lane insertion loss specified at the end of the 2000th physical insertion.

The module is without any cold-solder and breakdown of active components, such as microcontroller and burners at the end of the 2000th temperature cycle.

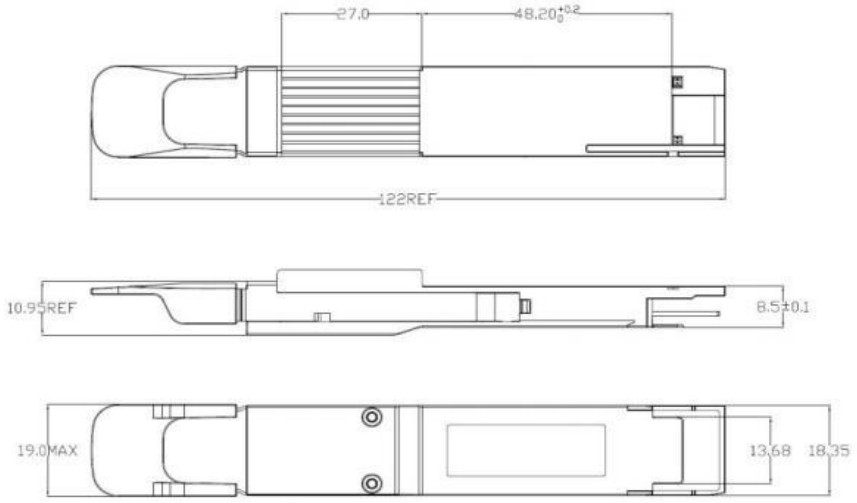
The value of guaranteed maximum insertion/temperature cycle saved in I2C registers in Page FFh, Address 252-253:

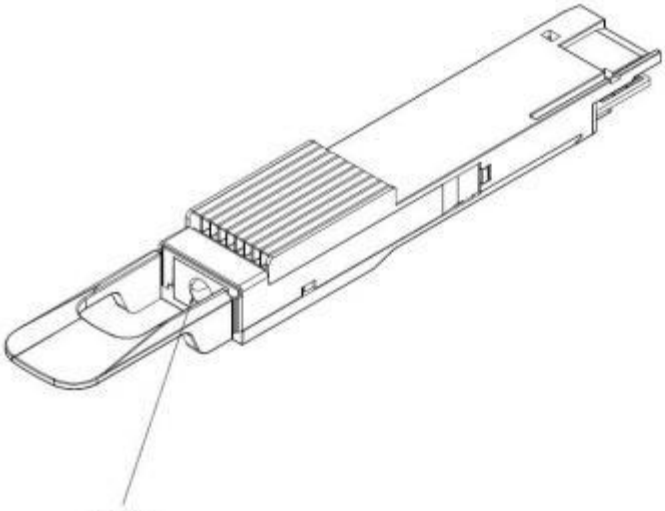
Table 11: Contact pads insertion cycle registers

Page	Address	Size	Name	Description	Type
FFh	252	1	Guaranteed maximum insertion/temperature cycle, MSB	Guaranteed maximum insertion/temperature cycle in hex. The goal is 2000 (07D0h) insertions.	RO
	253	1	Guaranteed maximum insertion/temperature cycle, LSB		RO

Package Outline

Dimensions are in millimeters. (Unit: mm





LED:
Solid green: low-power mode
Solid red: high-power mode
Blinking green: low-power mode with any of the interrupt flag is set
Blinking red: high-power mode with any of the interrupt flag is set