POQD40VR4	Pro-optics 400G OSFP112 VR4 transceiver, MPO-12 APC interface, 850nm, up to 50m with OM4, Pull tab

Key Features

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- OSFP form factor hot pluggable
- CMIS compliance
- 4 parallel lanes of 100G-PAM4 electrical and optical parallel lanes
- optical port of MPO-12/APC
- Up to 50m reach on multi-mode fiber OM4 and 30m on OM3 with FEC
- 9 Watts max
- Case temperature range of 0°C to 70°C

Applications

The transceiver is designed for Ethernet, Telecom and Infiniband use cases. The application advertisements listed below allow host software to select proper application following CMIS definition

- Application case 1, 1x400G VR4, 1 of 400G per port point to point connections.
- Application case 2, 4x100G VR, 4 of 100G per channel breakout

connections. Table 1 shows CMIS application advertisements list:

Table 1. CMIS Application advertisements

ApSel Code	Host Electrical Interface	Module Media Interface	Host and Media Lane Count	Host Lane Assignment
ApSel 1	4F(400GAUI-4-S C2M)	1F (400GBASE-VR4)	44 (4:4)	01 (lanes 1)
ApSel 2	4B(100GAUI-1-S C2M)	1D(100GBASE-VR)	11 (1:1)	03 (lanes 1,2)

Introduction

This product is an 400Gb/s Octal Small Form-factor Pluggable (OSFP) optical module without top open fin designed for 50m with OM4 fiber optical communication applications. The module converts 4 channels of 100Gb/s (PAM4) electrical input data to 4 channels of parallel optical signals, each capable of 100Gb/s operation for an aggregate data rate of 400Gb/s. Reversely, on the receiver side, the module converts 4 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 400Gb/s into 4 channels of 100Gb/s (PAM4) electrical output data.

MPO-12 connector can be plugged into the OSFP112 VR4 module jack with 4 channels. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

I2C interface is supported to read and control the status of this product.

Figure 1 shows the transceiver block diagram

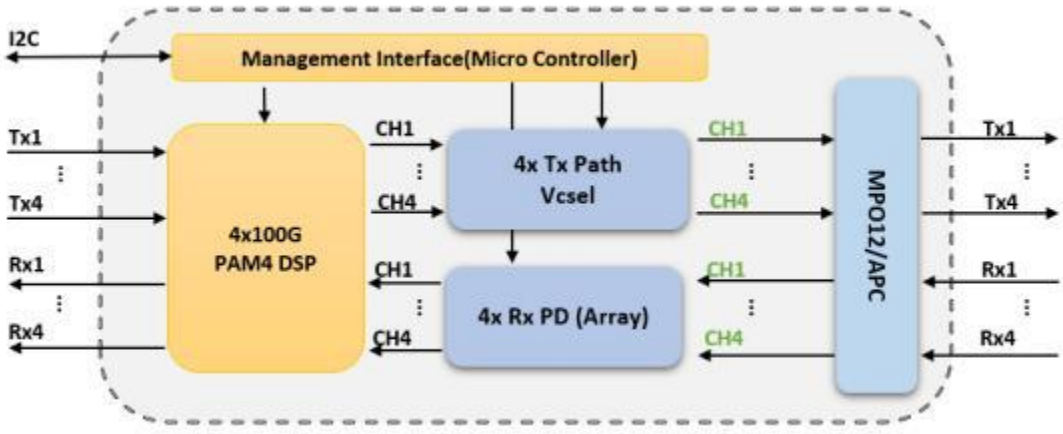

Figure 1. Transceiver Block Diagram

Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 8.1 of OSFP MSA Specification.

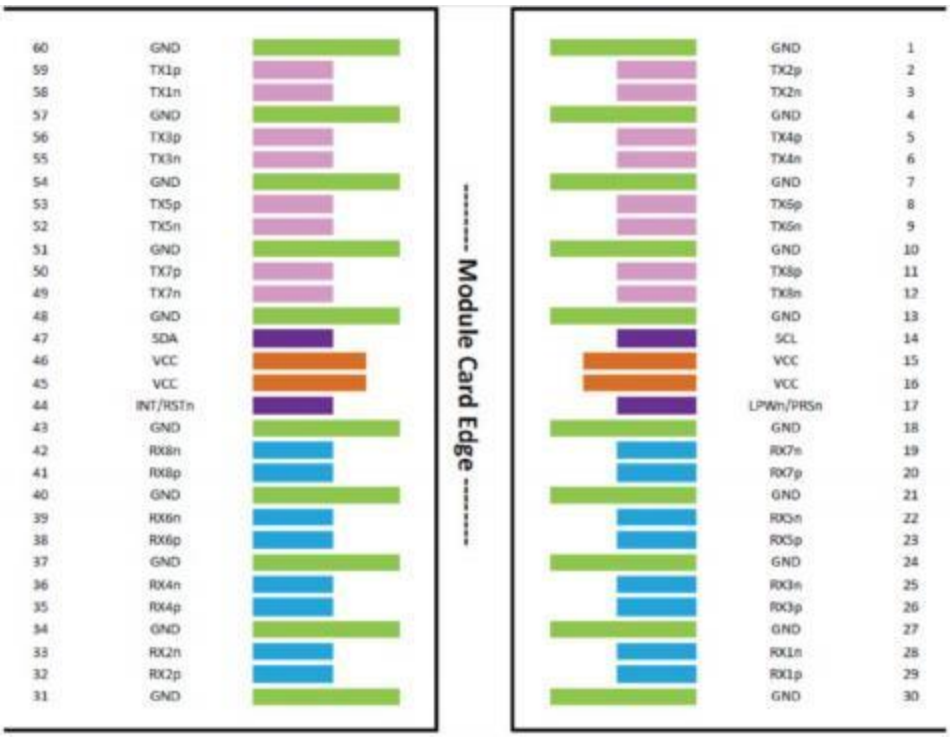

Figure 2. MSA Compliant Connector

Table 2 shows the detailed pin list

Table 2 OSFP connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML- I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML- I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML- I	Input from Host	3

9	TX6n	Transmitter Data Inverted	CML- I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML- I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi- Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non- Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non- Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non- Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non- Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non- Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non- Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non- Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1
41	RX8p	Receiver Data Non- Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi- Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML- I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
51	GND		Ground		1

52	TX5n	Transmitter Data Inverted	CML- I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML- I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML- I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML- I	Input from Host	3
60	GND		Ground		1

Table 3 shows the detailed control pins

Table 3. OSFP Control pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/PRSn	Input/Output	Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3.
INT/RSTn	Input/Output	Dual Funtion Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3.

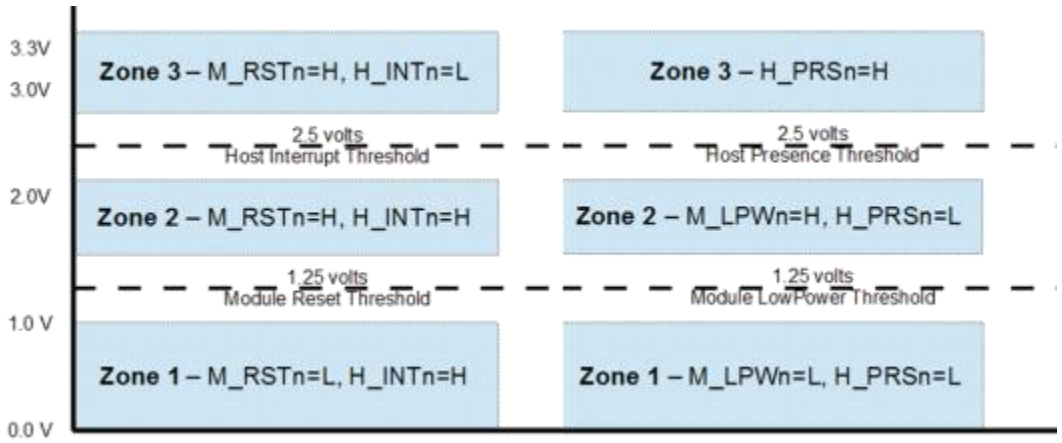

Figure 3. Voltage Zones

Figure 4 shows the recommended power supply filter design

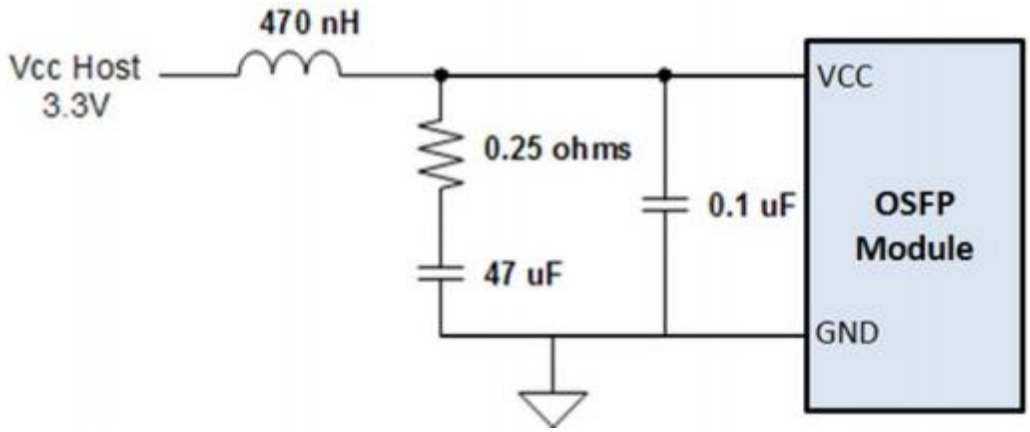

Figure 4. Recommended Power Supply Filter

Optical Port Description

The optical interface port is MPO-12 receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.

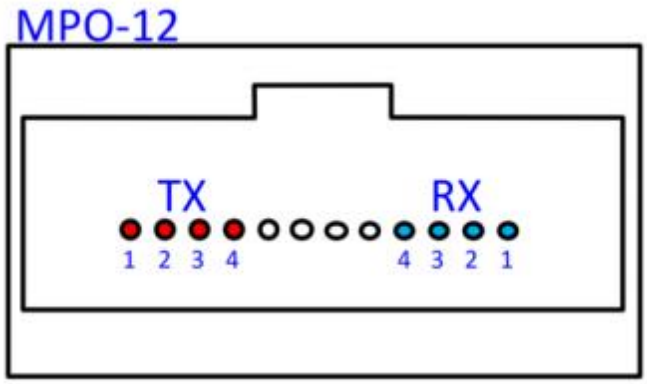

Figure 5. Optical Media Dependent Interface port assignments

Specification

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			53.125		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance (OM4)	D1	2		50	m	2
Link Distance (OM3)	D2	2		30	m	

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				9.0	W	
Supply Current	Icc			2.87	A	
Module Input (each Lane)						
Signaling Rate, each Lane	TP1	53.125 ± 100 ppm			GBd	
Differential pk-pk voltage tolerance	TP1a	750			mV	
Peak-to-peak AC common- mode voltage tolerance Low-frequency,VCM_{LF} Full-band,VCM_{FB}	TP1a	32 80			mV	
Differential-mode to common-mode return loss, RLcd	TP1	IEEE 802.3ck Equation (120G – 2)			dB	
Effective return loss, ERL	TP1	8.5			dB	
Differential termination mismatch	TP1			10	%	

Module stressed input tolerance	TP1a	IEEE802.3ck 120G.3.4.3				
Single-ended voltage tolerance range	TP1a	– 0.4 to 3.3			V	

DC common-mode voltage tolerance Upper limit Lower limit	TP1			2.85 –0.35	V V	
Receiver (each Lane)						
Signaling Rate, each lane	TP4			53.125 ± 100 ppm	GBd	
Peak-to-peak AC common- mode voltage Low-frequency, VCM_{LF} Full-band, VCM_{FB}	TP4			 32 80	mV	
Differential peak-to-peak output voltage Short mode Long mode	TP4			 600 845	 mV mV	
Eye height	TP4	15			mV	
Vertical eye closure, VEC	TP4			12	dB	
Common-mode to differential-mode return loss, RLdc	TP4	IEEE802.3ck Equation (120G– 1)			dB	
Effective return loss, ERL	TP4	8.5			dB	
Differential termination mismatch	TP4			10	%	
Transition time	TP4	8.5			ps	
DC common-mode voltage tolerance Upper limit Lower limit	TP4			2.85 -0.35	V V	

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format		PAM4				
Wavelength	λ	842		948	nm	
RMS spectral width				0.65	nm	1
Average Launch Power, each Lane	P_{AVG}	-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	P_{OMA}	-2.6(For max (TECQ, TDECQ) ⩽ 1.8 dB) -4.4 + max(TECQ,TDECQ) (For 1.8 < max (TECQ, TDECQ) ⩽ 4.4 dB)		3.5	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane	TDECQ			4.4	dB	
Transmitter eye closure for PAM4, each Lane	TECQ			4.4	dB	
Overshoot/undershoot				29	%	
Transmitter power excursion, each Lane				2.3	dBm	
Extinction Ratio	ER	2.5			dB	
Transition Time	T_t			17	ps	
Average Launch Power of OFF Transmitter, each Lane	P_{off}			-30	dBm	
RIN_{14} OMA	RIN			-132	dB/Hz	
Optical Return Loss Tolerance	TOL			14	dB	
Encircled flux		⩾ 86% at 19 μm ⩽ 30% at 4.5 μm				2
Receiver						
Data Rate, each Lane		53.125 ± 100 ppm			GBd	

Modulation Format		PAM4				
Center wavelength	λ	842		948	Nm	
Damage Threshold, each Lane	TH_d	5			dBm	3
Average Receive Power, each Lane		-6.3		4	dBm	4
Receive Power (OMA_{outer}), each Lane				3.5	dBm	
Receiver Reflectance	R_R			-15	dB	
Receiver Sensitivity (OMA_{outer}), each Lane	SEN			-4.4(For TECQ ≤ 1.8 dB) – 6.2 + TECQ （For 1.8＜TECQ ≤ 4.4 dB)	dBm	5
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-1.8	dBm	6
LOS Assert	LOSA	-15			dBm	
LOS De-assert	LOSD			-9.2	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Conditions of Stress Receiver Sensitivity Test (Note 7)						
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			4.4		dB	
OMA_{outer} of each aggressor lane			3.5		dBm	

Notes:

1. RMS spectral width is the standard deviation of the spectrum.
2. If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280- 1-4.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

5. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of TECQ up to 4.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 5.

$$RS = \max(-4.4, TECQ - 6.2)\ \text{dBm} \quad (1)$$

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

6. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4}.

7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

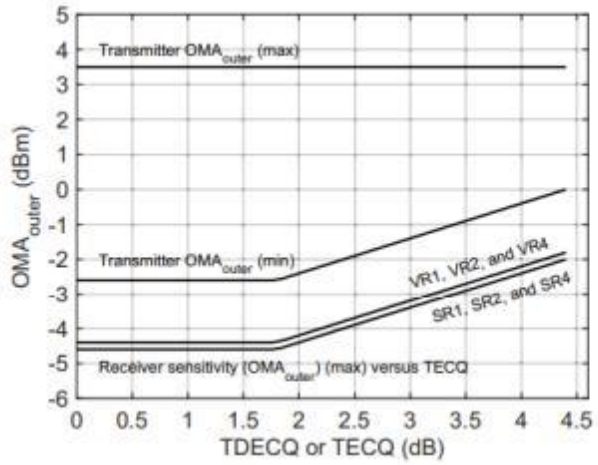

Figure 6. Illustration of Receiver Sensitivity Mask for 400G-VR4

Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	

Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Mechanical Drawing

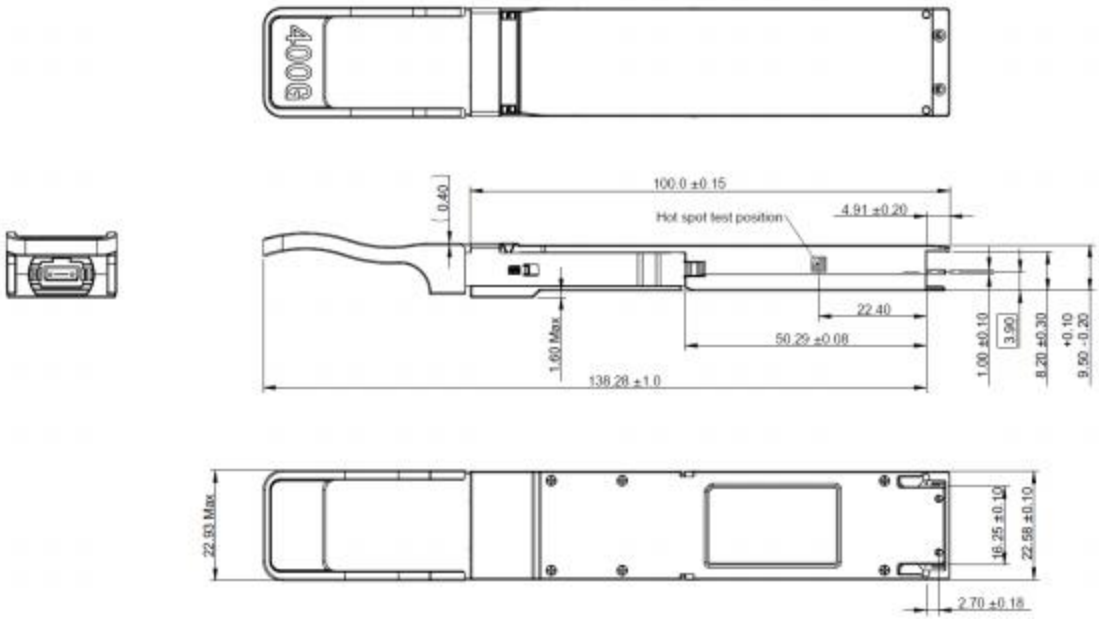

Figure 7. Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.