# 800G OSFP112 2xFR4 Optical Transceiver

## POOS80FR8

**Part Number Ordering Information**

| | |
|---|---|
| POOS80FR8 | Pro-optics 800G OSFP112 2xFR4 transceiver, dual duplex LC Interface, 4 CWDM Lanes, up to 2km, Top-closed-fin, Pull tab |

## Table of Content

## 1. Introduction

This product is an 800Gb/s Octal Small Form-factor Pluggable (OSFP) optical module with top closed fin designed for 2km optical communication applications. The module converts 8 channels of 100Gb/s (PAM4) electrical input data to 2 sets of 4 CWDM optical signals and multiplexes them into 2 sets of a single channel for 425Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes 2 sets of a single channel 425Gb/s signal inputs into 2 sets of 4 CWDM channel signals and converts them to 8 output channels of 106Gb/s electrical data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains an optical Dual SMF LC duplex connector for the optical interface and a 60-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission.

I2C interface is supported to read and control the status of this product.

Figure 1 shows the transceiver block diagram

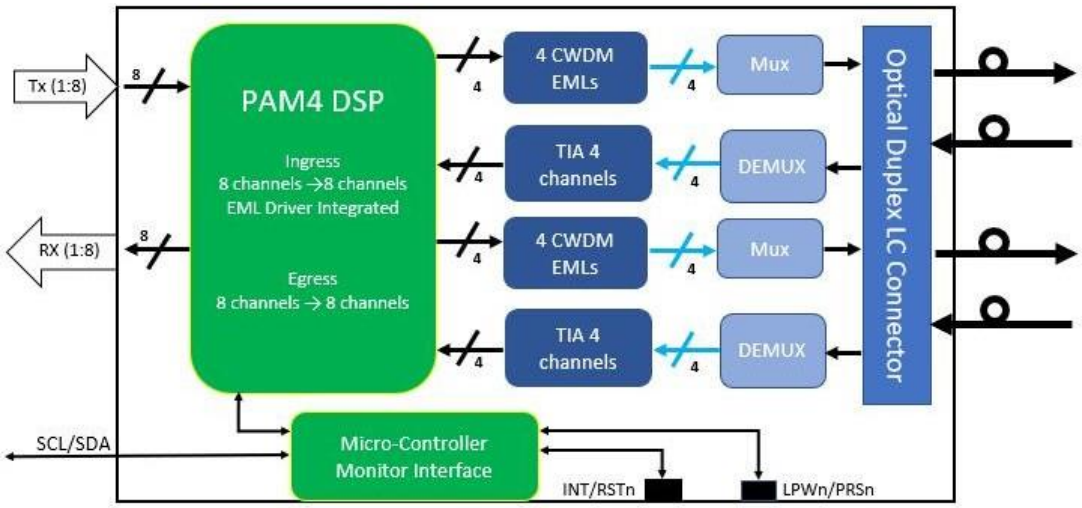


**Figure 1. Transceiver Block Diagram**

- OSFP form factor hot pluggable
- Top closed fin
- 2 sets of 4 CWDM lanes MUX/DEMUX design
- Electrical Interface: compliant to 800GAUI-8(8x106.25Gb/s) in IEEE 802.3ck
- Optical Interface: compliant to 400G-FR4 technical specification
- 16 Watts max
- CMIS compliance
- Case temperature range of 0°C to 70°C
- Dual SMF LC duplex connectors (5.25mm pitch)
- Up to 2km over SMF with KP4 FEC on host side

## 2. Key Features

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

## 3. Applications

The transceiver is designed for Ethernet, Telecom and Infiniband use cases. The application advertisements listed below allow host software to select proper application following CMIS definition

- Application case 1, 2x400G FR4, 2 sets of 400G per port breakout connections.
- Application case 2, 2x200G FR4, 2 sets of 200G per port breakout connections.
- Application case 3, 8x100G FR, 8 of 100G per port breakout connections.
- Application case 4, 1x800G FR8, 1 of 800G per port point to point connection.
- Applications for backward compliance, refer to detailed application list below.

Mixed applications of case 1 and case 3 are also supported.

Table 1 shows CMIS application advertisements list:

**Table 1. CMIS Application advertisements**

| ApSel Code | Host Electrical Interface | Module Media Interface | Host and Media Lane Count | Host Lane Assignment |
|---|---|---|---|---|
| ApSel 1 | 50(400GAU1-4-L C2M) | 1D(400GBASE-FR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 2 | 32(IB NDR) | 1D(400GBASE-FR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 3 | 0F(200GAU1-4 C2M) | 18(200GBASE-FR4) | 44(4:4) | 11 (lanes 1,5) |
| ApSel4 | 31(IB HDR) | 18(200GBASE-FR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 5 | 4C(100GAU1-1-L C2M) | 15(100GBASE-FR1) | 11(1:1) | FF (lane 1,2,3,4,5,6,7,8) |
| ApSel 6 | 52(800G L C2M) | 0(Undefined) | 88(1:1) | 01 (lanes 1) |
| ApSel 7 | 4F(400GAU1-4-S C2M) | 1D (400GBASE-FR4) | 44(4:4) | 11 (lanes 1,5) |
| ApSel 8 | 4B(100GAU1-1-S C2M) | 15(100GBASE-FR1) | 11(1:1) | FF (lane 1,2,3,4,5,6,7,8) |
| ApSel 9 | 51(800G S C2M) | 0 (Undefined) | 88 (1:1) | 01 (lanes 1) |
| ApSel 10 | 42(100CAU-4 FEC) | 10(100G CWDM4 MSA) | 44(4:4) | 11 (lanes 1,5) |
| ApSel 11 | 30(IB EDR) | 10(100G CWDM4 MSA) | 44(4:4) | 11 (lanes 1,5) |

## 4. Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 8.1 of OSFP MSA Specification.

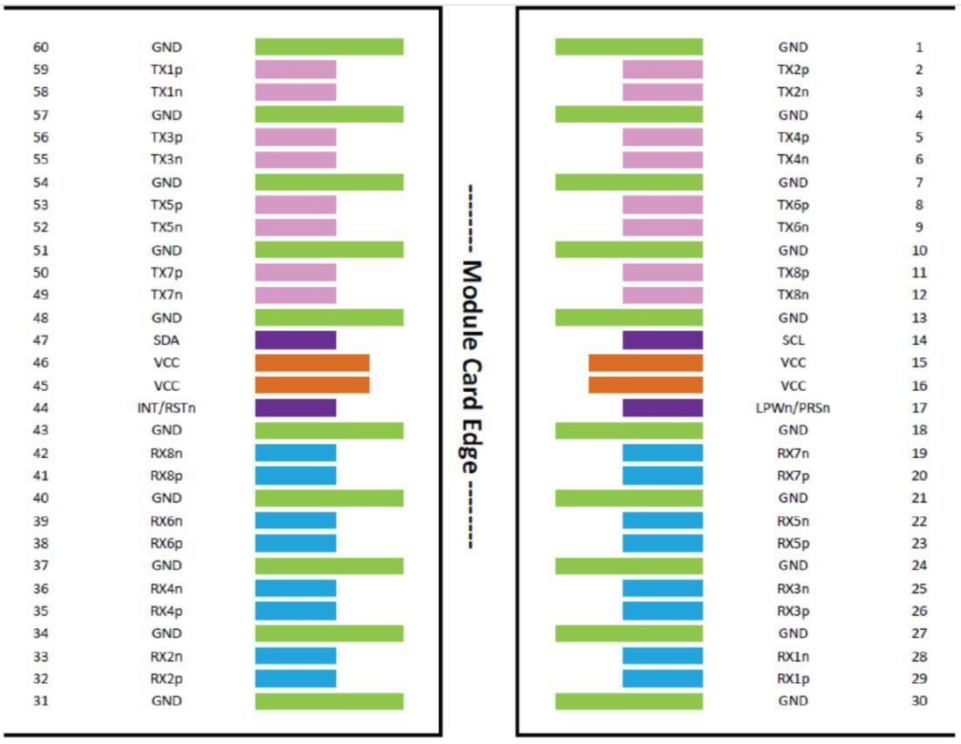


**Figure 2. MSA Compliant Connector**

Table 2 shows the detailed pin list

Table 2 OSFP connector pin list

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence |
|---|---|---|---|---|---|
| 1 | GND | | Ground | | 1 |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 4 | GND | | Ground | | 1 |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 7 | GND | | Ground | | 1 |
| 8 | TX6p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 10 | GND | | Ground | | 1 |
| 11 | TX8p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 12 | TX8n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 13 | GND | | Ground | | 1 |
| 14 | SCL | 2-wire Serial interface clock | LVCMOS-I/O | Bi-directional | 3 |
| 15 | VCC | +3.3V Power | | Power from Host | 2 |
| 16 | VCC | +3.3V Power | | Power from Host | 2 |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 |
| 18 | GND | | Ground | | 1 |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 21 | GND | | Ground | | 1 |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 24 | GND | | Ground | | 1 |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 27 | GND | | Ground | | 1 |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 30 | GND | | Ground | | 1 |
| 31 | GND | | Ground | | 1 |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 34 | GND | | Ground | | 1 |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 37 | GND | | Ground | | 1 |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 40 | GND | | Ground | | 1 |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 43 | GND | | Ground | | 1 |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 |
| 45 | VCC | +3.3V Power | | Power from Host | 2 |
| 46 | VCC | +3.3V Power | | Power from Host | 2 |
| 47 | SDA | 2-wire Serial interface data | LVCMOS-I/O | Bi-directional | 3 |
| 48 | GND | | Ground | | 1 |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 51 | GND | | Ground | | 1 |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 |

| | | | | | |
|---|---|---|---|---|---|
| 53 | TX5p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 54 | GND | | Ground | | 1 |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 57 | GND | | Ground | | 1 |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 60 | GND | | Ground | | 1 |

Table 3 shows the detailed control pins

Table 3. OSFP Control pins

| Name | Direction | Description |
|---|---|---|
| SCL | BiDir | 2-wire serial clock signal. Requires pull-up resistor to 3.3V on host |
| SDA | BiDir | 2-wire serial data signal. Requires pull-up resistor to 3.3V on host. |
| LPWn/PRSn | Input/Output | Dual Function Signal<br>. Low Power mode is an active-low input signal<br>. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal<br>Voltage zones is shown as figure3. |
| INT/RSTn | Input/Output | Dual Funtion Signal<br>. Reset is an active-low input signal<br>. Interrupt is an active-high output signal<br>Voltage zones is shown as figure 3. |

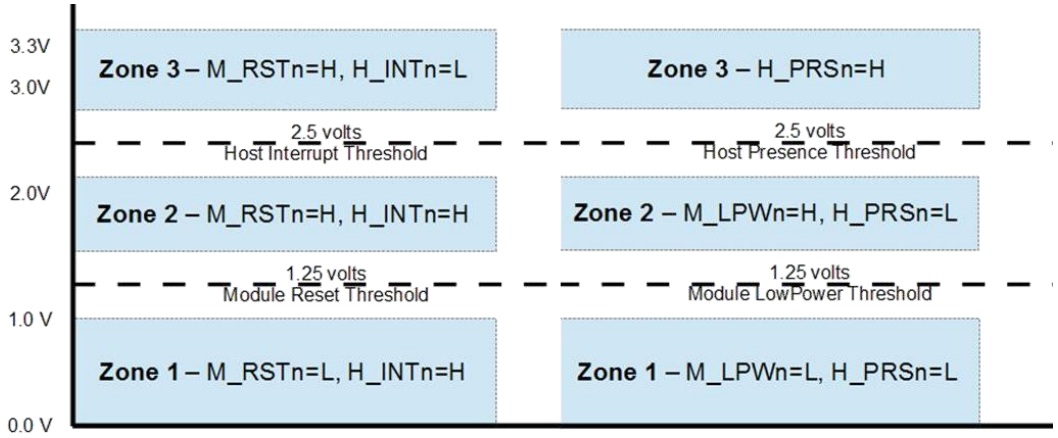


**Figure 3. Voltage Zones**

Figure 4 shows the recommended power supply filter design

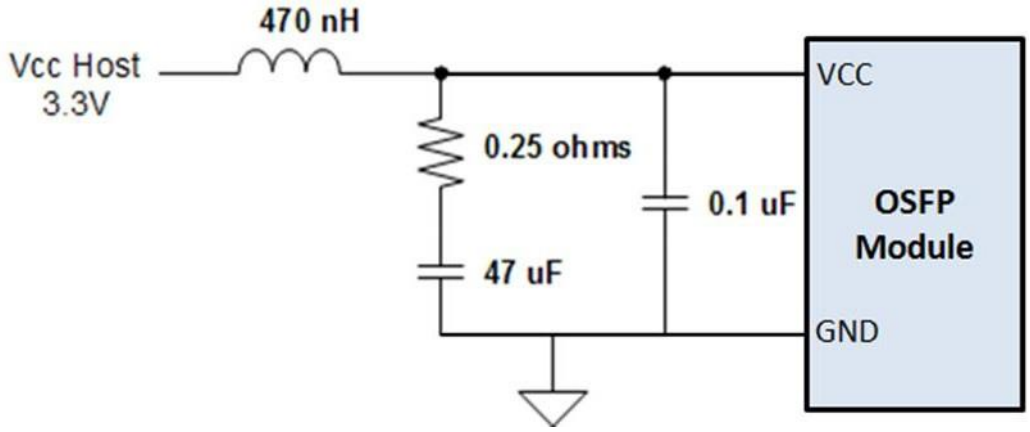


**Figure 4. Recommended Power Supply Filter**

## 5. Optical Port Description

The optical interface port is dual duplex LC. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.

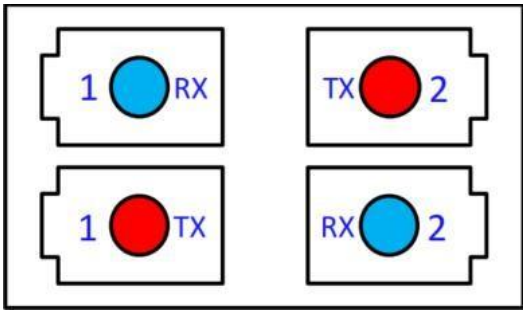


**Figure 5. Optical Media Dependent Interface port assignments**

## 6. Specification

### 6.1 Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | -40 | 85 | degC | |
| Operating Case Temperature | $T_{OP}$ | 0 | 70 | degC | |
| Power Supply Voltage | $V_{CC}$ | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |

## 6.2 Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Operating Case Temperature | $T_{OP}$ | 0 | | 70 | degC | |
| Power Supply Voltage | $V_{CC}$ | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 53.125 | | GBd | PAM4 |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | $2.4x10^{-4}$ | | |
| Post-FEC Bit Error Ratio | | | | $1x10^{-15}$ | | 1 |
| Link Distance | D | 2 | | 2000 | m | 2 |

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

## 6.3 Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Test Point | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Power Consumption | | | | 16 | W | |
| Supply Current | Icc | | | 4.84 | A | |
| **Module Input (each Lane)** | | | | | | |
| Signaling Rate, each Lane | TP1 | 53.125 ± 100 ppm | | | GBd | |
| DC Common-mode input Voltage | TP1 | -0.35 | | 2.85 | V | |
| Single-ended input Voltage | TP1a | -0.4 | | 3.3 | V | |
| AC Common-mode RMS input Voltage<br>Low-frequency,$VCM_{LF}$<br>Full-Band,$VCM_{LF}$ | TP1a | <br>32<br>80 | | | mV | |
| Module stressed input test | | IEEE 802.3ck 120G3.4.3 | | | | |
| Differential Peak-to-Peak input Voltage tolerance | TP1a | 750 | | | mV | |
| Common to Different Mode input Return Loss | TP1 | IEEE802.3ck Equation 120G-2 | | | | |
| Effective input Return Loss | TP1 | 8.5 | | | dB | |
| Differential input Termination Mismatch | TP1 | | | 10 | % | |
| **Module Output (each Lane)** | | | | | | |
| Signaling Rate, each lane | TP4 | 53.125 ± 100 ppm | | | GBd | |
| Differential Peak-to-Peak | TP4 | | | | mV | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Output Voltage<br>Short mode<br>Long mode | | | | <br>600<br>845 | | |
| AC Common Mode Output Voltage, RMS<br>Low-frequency,$VCM_{LF}$<br>Full-Band,$VCM_{LF}$ | TP4 | | | <br>32<br>80 | mV | |
| Differential Termination Mismatch | TP4 | | | 10 | % | |
| Eye height | TP4 | 15 | | | mV | |
| Vertical eye closure, VEC | TP4 | | | 12 | dB | |
| Common-mode to Differential mode output Return Loss | TP4 | IEEE802.3ck Equation 120G-1 | | | dB | |
| Effective output Return Loss | TP4 | 8.5 | | | dB | |
| Output Transition time (20% to 80%) | TP4 | 8.5 | | | ps | |
| DC Common-mode output Voltage | TP4 | -350 | | 2850 | mV | |
| Differential termination mismatch | TP4 | | | 10 | % | |

## 6.4 Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Wavelength Assignment | L0 | 1264.5 | 1271 | 1277.5 | nm | |
| | L1 | 1284.5 | 1291 | 1297.5 | nm | |
| | L2 | 1304.5 | 1311 | 1317.5 | nm | |
| | L3 | 1324.5 | 1331 | 1337.5 | nm | |
| | L4 | 1264.5 | 1271 | 1277.5 | nm | |
| | L5 | 1284.5 | 1291 | 1297.5 | nm | |
| | L6 | 1304.5 | 1311 | 1317.5 | nm | |
| | L7 | 1324.5 | 1331 | 1337.5 | nm | |
| **Transmitter** | | | | | | |
| Data Rate, each Lane | | 53.125 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | |
| Total average launch power | | | | 9.5 | dBm | |
| Average Launch Power, each Lane | $P_{AVG}$ | -3.2 | | 3.5 | dBm | 1 |
| Outer Optical Modulation | $P_{OMA}$ | Max(-0.2,- | | 3.7 | dBm | 2 |

| | | | | | | |
|---|---|---|---|---|---|---|
| Amplitude ($OMA_{outer}$), each Lane | | 1.6+TDECQ) | | | | |
| Difference in launch power between any two lanes ($OMA_{outer}$) | | | | 4 | dB | |
| Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane | TDECQ | | | 3.4 | dB | |
| Transmitter eye closure for PAM4 (TECQ), each Lane | TECQ | | | 3.4 | dB | |
| \|TDECQ-TECQ\| | | | | 2.5 | dB | |
| Over/under-shoot | | | | 22 | % | |
| Transmitter peak-to-peak power | | | | 4.5 | dBm | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| $RIN_{17.1}OMA$ | RIN | | | -136 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 17.1 | dB | |
| Transmitter Reflectance | $R_T$ | | | -26 | dB | |
| Transmitter Transition Time | | | | 17 | ps | |
| Average Launch Power of OFF Transmitter, each Lane | $P_{off}$ | | | -16 | dBm | |
| **Receiver** | | | | | | |
| Data Rate, each Lane | | 53.125 ± 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Damage Threshold, each Lane | $TH_d$ | 4.5 | | | dBm | 3 |
| Average Receive Power, each Lane | | -7.2 | | 3.5 | dBm | 4 |
| Receive Power ($OMA_{outer}$), each Lane | | | | 3.7 | dBm | |
| Difference in receive power between any two lanes ($OMA_{outer}$) | | | | 4.1 | dB | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Receiver Sensitivity ($OMA_{outer}$), each Lane | SEN | | | Equation (1) | dBm | 5 |
| Stressed Receiver Sensitivity ($OMA_{outer}$), each Lane | SRS | | | -2.6 | dBm | 6 |
| Receiver Reflectance | $R_R$ | | | -26 | dB | |
| LOS Assert | LOSA | -15 | | -10.5 | dBm | |
| LOS De-assert | LOSD | | | -7.5 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| **Conditions of Stress Receiver Sensitivity Test (Note 7)** | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | | 3.4 | | dB | |
| $OMA_{outer}$ of each aggressor lane | | | 1.5 | | dBm | |

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for $OMA_{outer}$(min) vary with TDECQ. Figure 6 illustrates this along with the values for $OMA_{outer}$(max).
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity ($OMA_{outer}$) is informative and is defined for a transmitter with a value of TECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 6.

$$S = \max(-4.6, TC - 6.0)\ B \quad (1)$$

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

6. Measured with conformance test signal at TP3 for the BER equal to $2.4 \times 10^{-4}$.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

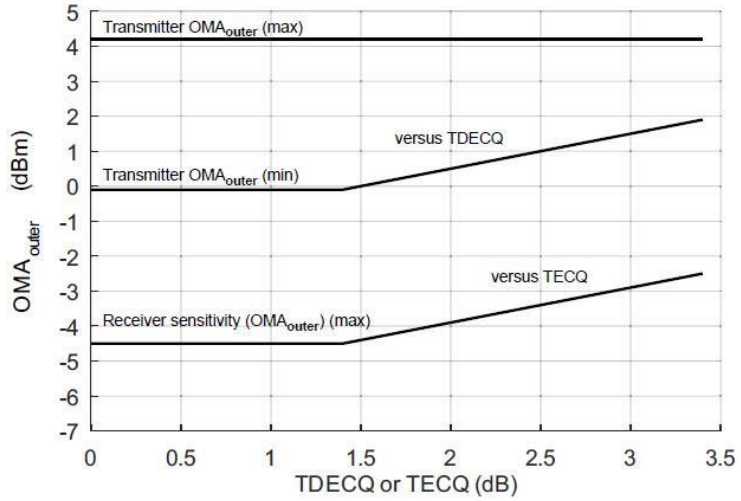


**Figure 6. Illustration of Transmitter OMA$_{outer}$ and Receiver Sensitivity Mask for 2x400G FR4**

## 6.5 Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI _VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

## 7. Mechanical Drawing

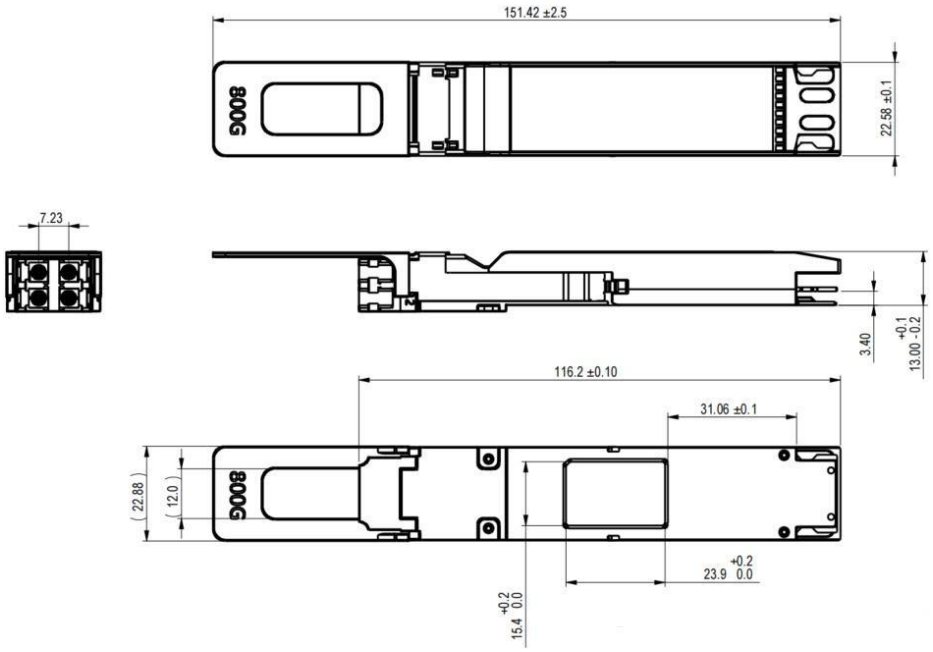


**Figure 7. Mechanical Outline**

## 8. ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## 9. Laser safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## 10. History Record

| Rev. No. | Date | Author(s) | Reviewer(s) | Comments |
|---|---|---|---|---|
| 1.0 | Feb/15/2023 | Dylan Qian | Vincent Ye | Released |
| 1.1 | June/5/2023 | Dylan Qian | Vincent Ye | Updated application codes |